The C701 Reverse Blocking Thyristor now has extended voltage blocking capability through unique multi-diffusion processing of 53 mm nominal silicon without sacrificing essential ratings and characteristics.

The C701 is designed specifically for phase control applications like DC motor control, power supplies, cycloconverters and load commutated inverters.

FEATURES

- Optimized pilot gate for high di/dt rating
- Excellent withstand to high dv/dt voltage fronts
- Enhanced surge and Igt ratings for fuse coordination
- Glazed-fluted ceramic with metal—metal welded seal 1.0 in., 25.4 mm creepage
  ¾ in., 15.9 mm clearance

MAXIMUM ALLOWABLE RATINGS

<table>
<thead>
<tr>
<th>TYPE</th>
<th>REPETITIVE PEAK OFF-STATE AND REVERSE VOLTAGE, ( V_{on}/V_{off} )</th>
<th>REPETITIVE PEAK OFF-STATE AND REVERSE VOLTAGE, ( V_{on}/V_{off} )</th>
<th>TRANSIENT PEAK REVERSE VOLTAGE (NON RECURRENT)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>( T_r = -40^\circ C ) TO +125^\circ C</td>
<td>( T_r = 0^\circ C ) TO 125^\circ C</td>
<td>( V_{on}&lt;5 ) MILLISEC., ( V_{on} )</td>
</tr>
<tr>
<td>C701PB</td>
<td>1200 VOLTS</td>
<td>1300 VOLTS</td>
<td>1300 VOLTS</td>
</tr>
<tr>
<td>C701PC</td>
<td>1300</td>
<td>1400</td>
<td>1400</td>
</tr>
<tr>
<td>C701PD</td>
<td>1400</td>
<td>1600</td>
<td>1600</td>
</tr>
<tr>
<td>C701PE</td>
<td>1500</td>
<td>1800</td>
<td>1800</td>
</tr>
<tr>
<td>C701PM</td>
<td>1600</td>
<td>1900</td>
<td>1900</td>
</tr>
<tr>
<td>C701PS</td>
<td>1700</td>
<td>2000</td>
<td>2000</td>
</tr>
<tr>
<td>C701PN</td>
<td>1800</td>
<td>2100</td>
<td>2100</td>
</tr>
<tr>
<td>C701PT</td>
<td>1900</td>
<td>2200</td>
<td>2200</td>
</tr>
<tr>
<td>C701L</td>
<td>2000</td>
<td>2300</td>
<td>2300</td>
</tr>
<tr>
<td>C701LA</td>
<td>2100</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C701LB</td>
<td>2200</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Average Forward Current, On-State @ \( T_{case} = 70^\circ C \). \( I_T(AV) \). .................................................. 1300A
Peak One-Cycle Surge On-State Current, ITSM .................................................. 8.3ms ................................. 20KA
10.0ms .................................................. 1.8KA

Maximum Repetitive Rate-of-Rise of Anode Current @ 1500V bias
(Switching Rates \( \leq 60 \) Hz; snubber discharge \( \leq 50A \); see required gate drive)
Igt (for fusing) (at 8.3 milliseconds)
Peak Gate Power Dissipation, PGM .................................................. 200 W @ 40\( \mu \)s pulse
Average Gate Power Dissipation, PG(AV) .................................................. 20W
Peak Reverse Gate Voltage, VGRM .................................................. 20V
Peak Gate Current .................................................. 15A
Storage Temperature, \( T_{STG} \) .................................................. -40°C to +150°C
Operating Temperature, \( T_J \) .................................................. -40°C to +125°C
Mounting Force Required .................................................. 5000 - 6000 lb.
22.4 - 26.7 KN

NOTE
1. Half sine pulse, 10ms MAXIMUM pulse width, non repetitive
   Assume presspak mounted to heat dissipator of less than 0.3 °C/W
   All ratings and tests in accordance with NEMA-EIA JEDEC Standard RS-397
### CHARACTERISTICS

<table>
<thead>
<tr>
<th>TEST</th>
<th>SYMBOL</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>UNITS</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak Reverse and Off-State Blocking Current</td>
<td>$I_{D_{RM}}$ and $I_{R_{RM}}$</td>
<td>–</td>
<td>10</td>
<td>15</td>
<td>mA</td>
<td>$T_J = +25^\circ C, V = V_{D_{RM}} = V_{R_{RM}}$</td>
</tr>
<tr>
<td>Peak Reverse and Off-State Blocking Current</td>
<td>$I_{D_{RM}}$ and $I_{R_{RM}}$</td>
<td>–</td>
<td>45</td>
<td>65</td>
<td>mA</td>
<td>$T_J = +125^\circ C, V = V_{D_{RM}} = V_{R_{RM}}$</td>
</tr>
<tr>
<td>Effective Thermal Resistance, Junction-to-Case</td>
<td>$R_{JC}$</td>
<td>–</td>
<td>–</td>
<td>.023</td>
<td>°C/Watt</td>
<td>Junction-to-Case – Double Side Cooled (DC)</td>
</tr>
<tr>
<td>Critical Linear Rate-of-Rise of Forward Blocking Voltage (Higher values may cause device switching)</td>
<td>$dv/dt$</td>
<td>500</td>
<td>–</td>
<td>–</td>
<td>V/μsec</td>
<td>$T_J = +125^\circ C, V_{D_{RM}} = .80$ Rated, Gate Gate Open.</td>
</tr>
<tr>
<td>Holding Current</td>
<td>$I_H$</td>
<td>–</td>
<td>–</td>
<td>500</td>
<td>mADC</td>
<td>$T_C = +25^\circ C$, Anode supply = 20 Vdc. Initial On-State Current = 500 amps.</td>
</tr>
<tr>
<td>Latching Current</td>
<td>$I_L$</td>
<td>–</td>
<td>–</td>
<td>1.5</td>
<td>ADC</td>
<td>$T_C = +25^\circ C$, Anode voltage = 24 Vdc. Load resistance 12 ohms max.</td>
</tr>
<tr>
<td>Delay Time</td>
<td>$t_d$</td>
<td>–</td>
<td>1.5</td>
<td>–</td>
<td>μsec</td>
<td>Switching From 300 Volts. 20 volt, 10 ohm Gate. 0.5 μsec Rise Time, $T_J = 25^\circ C$</td>
</tr>
<tr>
<td>Gate Pulse Width Necessary to Trigger</td>
<td>–</td>
<td>–</td>
<td>10</td>
<td>3 μsec</td>
<td>0.5A, 15V minimum to support ratings</td>
<td></td>
</tr>
<tr>
<td>Gate Trigger Current nonoperational</td>
<td>$I_{GT}$</td>
<td>60</td>
<td>150</td>
<td>5.0</td>
<td>mADC</td>
<td>$T_C = 25^\circ C$, $V_D = 10$ Vdc, $R_L = 3$ ohms</td>
</tr>
<tr>
<td>Gate Trigger Voltage nonoperational</td>
<td>$V_{GT}$</td>
<td>–</td>
<td>2.5</td>
<td>4.5</td>
<td>Vdc</td>
<td>$T_C = +125^\circ C$, $V_D = .5$ x Rated, $R_L = 1000$ ohms</td>
</tr>
<tr>
<td>Peak On-State Voltage</td>
<td>$V_{TM}$</td>
<td>–</td>
<td>–</td>
<td>1.21</td>
<td>Volts</td>
<td>$T_C = 1000A$, $T_J = 125^\circ C$</td>
</tr>
<tr>
<td>Circuit Commutated Turn-Off Time</td>
<td>$t_q$</td>
<td>1000</td>
<td>125</td>
<td>250</td>
<td>μsec</td>
<td></td>
</tr>
</tbody>
</table>
| Suppressible Surge Current                            | $I_{TM(SUP)}$ | –    | 18   | –    | KA   | (1) $T_C = +125^\circ C$  
(2) $I_T = 1000$ Amps.  
(3) $V_R = 75$ Volts min.  
(4) 0.5 $V_{D_{RM}}$ Reapplied  
(5) Rate-of-rise of reapplied forward blocking voltage = 50V/μsec. (linear)  
(6) Gate bias during turn-off interval, Duty cycle ≤ 0.01%  
(7) $V_R$ .67 $V_{R_{RM}}$ Applied, 8.3 msec after completion of surge. (see waveforms below) |
Thyristor Gate Impedance
- This is enhanced by fast rising gate voltage, increasing anode bias and temperature.
- It is shown at a minimum for dc voltage, zero bias and low temperature.
- It is shown at a maximum for operating bias and recommended gate drive.

Gate Supply
- The short circuit current rise time should be approximately 0.5 \mu s and the duration longer than the delay time expected for the thyristor.

Minimum Acceptable Gate Current
- The intersection of load line and gate characteristic (encircled) indicates the minimum value of actual current flowing into the gate that is required during the delay time interval needed for the published dV/dt and snubber discharge ratings.

NOTES:
1. Add .006°C/W to account for both case to dissipator interfaces when properly mounted; e.g., RθjS = .028°C/W. See Mounting Instructions.

2. DC Thermal Impedance is based on average full cycle junction temperature. Instantaneous junction temperature may be calculated using the following modifications:
   - end of conducting portion of cycle
     - 120° sq. wave add .0025°C/W along entire curve
     - 180° sq. wave add .0018°C/W along entire curve
     - 180° sine wave add .0010°C/W along entire curve
   - end of full cycle
     - any wave, subtract .001°C/W along entire curve.
1. Maximum allowable heatsink temperature for sinusoidal current waveform – double-side cooling

2. Maximum allowable heatsink temperature for rectangular current waveform – double-side cooling

3. Maximum allowable heatsink temperature – circuit phase current waveform – double-side cooling

4. Average forward power dissipation for sinusoidal current waveform

5. Forward power dissipation for rectangular current waveform

6. Average forward power dissipation
NOTES:

Code: — — Non-Repetitive High Gate Drive
Repetitive High Gate Drive

High Gate Drive

Source
20V/10 ohms

Pulse Width, \( t_p \)
\( > 10 \mu s \)

Current Rise Time, \( t_r \)
\( < 0.5 \mu s \)

*Permissible circuit di/dt excluding snubber discharge. Repetitive di/dt is SPCD recommended maximum condition to achieve most industrial requirements for service life. It meets or exceeds the JEDEC test requirements for certification set forth in NEMA Std. Sk. 516 (1972). Non-repetitive di/dt meets the JEDEC 5 second rating.

**Snubber discharge, \( t_d \), is treated separately using the minimum value of snubber resistance indicated. This applies for long industrial life (20 – 30 years) in combination with circuit di/dt.

ALLOWABLE DI/DT AND SNUBBER RESISTANCE

PEAK RECOVERY CURRENT

NON-REPEETITIVE \( I_{TSW} \) AND \( I^2t \) CAPABILITY FOR FUSE COORDINATION

OUTLINE DRAWING

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USA