DESCRIPTION

The REF102 is a precision 10V voltage reference. The drift is laser-trimmed to 2.5ppm/°C max (CM grade) over the industrial temperature range and 5ppm/°C max (SM grade) over the military temperature range. The REF102 achieves its precision without a heater. This results in low power, fast warm-up, excellent stability, and low noise. The output voltage is extremely insensitive to both line and load variations and can be externally adjusted with minimal effect on drift and stability. Single supply operation from 11.4V to 36V and excellent overall specifications make the REF102 an ideal choice for demanding instrumentation and system reference applications.
## SPECIFICATIONS

### ELECTRICAL

At $T_A = +25^\circ C$ and $V_S = +15V$ power supply, unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>REF102A, R</th>
<th>REF102B, S</th>
<th>REF102C, M</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUTPUT VOLTAGE</td>
<td>Initial $T_A = 25^\circ C$</td>
<td>9.99</td>
<td>10.01</td>
<td>9.995</td>
<td>10.005</td>
</tr>
<tr>
<td>vs Temperature $^{(1)}$</td>
<td></td>
<td>10</td>
<td>10</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>vs Supply Line Regulation</td>
<td>$V_S = 11.4V$ to 36V</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>vs Output Current Load Regulation</td>
<td>$I_L = 0mA$ to +10mA</td>
<td>20</td>
<td>10</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>vs Time $T_A = 25^\circ C$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>vs Output Current Time</td>
<td>$T_A = 25^\circ C$</td>
<td>5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>P, U Packages $^{(2)}$</td>
<td></td>
<td>20</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Trim Range $^{(3)}$</td>
<td></td>
<td>±3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Capacitive Load, max</td>
<td></td>
<td>1000</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NOISE</td>
<td>(0.1Hz to 10Hz)</td>
<td>5</td>
<td>*</td>
<td>*</td>
<td>*</td>
</tr>
<tr>
<td>INPUT VOLTAGE RANGE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>INPUT VOLTAGE RANGE</td>
<td>+11.4</td>
<td>+36</td>
<td>*</td>
<td>*</td>
<td>*</td>
</tr>
<tr>
<td>QUIESCENT CURRENT</td>
<td>(I_{OUT} = 0)</td>
<td>+1.4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WARM-UP TIME $^{(4)}$</td>
<td>(To 0.1%)</td>
<td>15</td>
<td>*</td>
<td>*</td>
<td>*</td>
</tr>
</tbody>
</table>

### NOTES:

1. The “box” method is used to specify output voltage drift vs temperature. See the Discussion of Performance section.
2. Typically 5ppm/1000hrs after 168hr powered stabilization.
3. Trimming the offset voltage affects drift slightly. See Installation and Operating Instructions for details.

※ Specifications same as REF102A/R.
ORDERING INFORMATION

<table>
<thead>
<tr>
<th>PRODUCT</th>
<th>PACKAGE</th>
<th>TEMPERATURE RANGE</th>
<th>MAX INITIAL ERROR (mV)</th>
<th>MAX DRIFT (ppm/°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>REF102AU</td>
<td>8-Pin SOIC</td>
<td>–25°C to +85°C</td>
<td>±10</td>
<td>±10</td>
</tr>
<tr>
<td>REF102AP</td>
<td>8-Pin Plastic DIP</td>
<td>–25°C to +85°C</td>
<td>±10</td>
<td>±10</td>
</tr>
<tr>
<td>REF102BP</td>
<td>8-Pin Plastic DIP</td>
<td>–25°C to +85°C</td>
<td>±5</td>
<td>±5</td>
</tr>
<tr>
<td>REF102AM</td>
<td>Metal TO-99</td>
<td>–25°C to +85°C</td>
<td>±10</td>
<td>±10</td>
</tr>
<tr>
<td>REF102BM</td>
<td>Metal TO-99</td>
<td>–25°C to +85°C</td>
<td>±5</td>
<td>±5</td>
</tr>
<tr>
<td>REF102CM</td>
<td>Metal TO-99</td>
<td>–25°C to +85°C</td>
<td>±2.5</td>
<td>±2.5</td>
</tr>
<tr>
<td>REF102RM</td>
<td>Metal TO-99</td>
<td>–55°C to +125°C</td>
<td>±10</td>
<td>±10</td>
</tr>
<tr>
<td>REF102SM</td>
<td>Metal TO-99</td>
<td>–55°C to +125°C</td>
<td>±5</td>
<td>±5</td>
</tr>
</tbody>
</table>

ABSOLUTE MAXIMUM RATINGS

- **Input Voltage**: +40V
- **Operating Temperature**
  - P,U: –25°C to +85°C
  - M: –55°C to +125°C
- **Storage Temperature Range**
  - P,U: –40°C to +85°C
  - M: –65°C to +150°C
- **Lead Temperature (soldering, 10s)**: +300°C (SOIC, 3s): +260°C
- **Short-Circuit Protection to Common or V+**: Continuous

PACKAGE INFORMATION

<table>
<thead>
<tr>
<th>PRODUCT</th>
<th>PACKAGE</th>
<th>PACKAGE DRAWING NUMBER(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>REF102AU</td>
<td>8-Pin SOIC</td>
<td>182</td>
</tr>
<tr>
<td>REF102AP</td>
<td>8-Pin Plastic DIP</td>
<td>006</td>
</tr>
<tr>
<td>REF102BP</td>
<td>8-Pin Plastic DIP</td>
<td>006</td>
</tr>
<tr>
<td>REF102AM</td>
<td>Metal TO-99</td>
<td>001</td>
</tr>
<tr>
<td>REF102BM</td>
<td>Metal TO-99</td>
<td>001</td>
</tr>
<tr>
<td>REF102CM</td>
<td>Metal TO-99</td>
<td>001</td>
</tr>
<tr>
<td>REF102RM</td>
<td>Metal TO-99</td>
<td>001</td>
</tr>
<tr>
<td>REF102SM</td>
<td>Metal TO-99</td>
<td>001</td>
</tr>
</tbody>
</table>

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

**ELECTROSTATIC DISCHARGE SENSITIVITY**

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.
TYPICAL PERFORMANCE CURVES

At $T_A = +25^\circ C$, $V_S = +15V$, unless otherwise noted.

POWER TURN-ON RESPONSE

POWER TURN-ON RESPONSE with 1µF Cn

LOAD REGULATION

POWER SUPPLY REJECTION vs FREQUENCY

QUIESCENT CURRENT vs TEMPERATURE

RESPONSE TO THERMAL SHOCK

REF102CM Immersed in +85°C Fluorinert Bath

QUIESCENT CURRENT vs TEMPERATURE
At $T_A = +25^\circ C$, $V_S = +15V$, unless otherwise noted.

**TYPICAL REF102 REFERENCE NOISE**

Low Frequency Noise (1s/div)
(See Noise Test Circuit)

**Noise Test Circuit.**

- DUT
- OPA27
- Oscilloscope
- Gain = 100V/V
- $f_{1/2}$ = 0.1Hz and 10Hz
- 20Ω
- 15.8kΩ
- 100µF
- 2µF
- 8kΩ
- 2kΩ

Noise Voltage ($\mu$V)
THEORY OF OPERATION

Refer to the diagram on the first page of this data sheet. The 10V output is derived from a compensated buried zener diode DZ1, op amp A1, and resistor network R1–R6.

Approximately 8.2V is applied to the non-inverting input of A1 by DZ1, R1, R2, and R3 are laser-trimmed to produce an exact 10V output. The zener bias current is established from the regulated output voltage through R4. R5 allows user-trimming of the output voltage by providing for small external adjustment of the amplifier gain. Because the TCR of R5 closely matches the TCR of R1, R2 and R3, the voltage trim has minimal effect on the reference drift. The output voltage noise of the REF102 is dominated by the noise of the zener diode. A capacitor can be connected between the Noise Reduction pin and ground to form a low-pass filter with R6 and roll off the high-frequency noise of the zener.

DISCUSSION OF PERFORMANCE

The REF102 is designed for applications requiring a precision voltage reference where both the initial value at room temperature and the drift over temperature are of importance to the user. Two basic methods of specifying voltage reference drift versus temperature are in common usage in the industry—the “butterfly method” and the “box method.” The REF102 is specified with the more commonly used “box method.” The “box” is formed by the high and low specification temperatures and a diagonal, the slope of which is equal to the maximum specified drift.

Since the shape of the actual drift curve is not known, the vertical position of the box is not exactly known either. It is, however, bounded by V_UPPER_BOUND and V_LOWER_BOUND (see Figure 1). Figure 1 uses the REF102CM as an example. It has a drift specification of 2.5ppm/°C maximum and a specification temperature range of -25°C to +85°C. The “box” height, V1 to V2, is 2.75mV.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CIRCUIT CONNECTION

Figure 2 shows the proper connection of the REF102. To achieve the specified performance, pay careful attention to layout. A low resistance star configuration will reduce voltage errors, noise pickup, and noise coupled from the power supply. Commons should be connected as indicated being sure to minimize interconnection resistances.

OPTIONAL OUTPUT VOLTAGE ADJUSTMENT

Optional output voltage adjustment circuits are shown in Figures 3 and 4. Trimming the output voltage will change the voltage drift by approximately 0.008ppm/°C per mV of trimmed voltage. The circuit in Figure 3, any mismatch in TCR between the two sections of the potentiometer will also affect drift, but the effect of the ΔTCR is reduced by a factor of five by the internal resistor divider. A high quality potentiometer, with good mechanical stability, such as a cermet, should be used. The circuit in Figure 3 has a minimum trim range of ±300mV. The circuit in Figure 4 has less range but provides higher resolution. The mismatch in TCR between R5 and the internal resistors can introduce some slight drift. This effect is minimized if R5 is kept significantly larger than the 50kΩ internal resistor. A TCR of 100ppm/°C is normally sufficient.
APPLICATIONS INFORMATION

High accuracy, extremely low drift, outstanding stability, and low cost make the REF102 an ideal choice for all instrumentation and system reference applications. Figures 6 through 14 show a variety of useful application circuits.

FIGURE 6. –10V Reference Using a) Resistor or b) OPA27.

OPTIONAL NOISE REDUCTION

The high-frequency noise of the REF102 is dominated by the zener diode noise. This noise can be greatly reduced by connecting a capacitor between the Noise Reduction pin and ground. The capacitor forms a low pass filter with $R_o$ (refer to the figure on the first page of the data sheet) and attenuates the high-frequency noise generated by the zener. Figure 5 shows the effect of a 1µF noise reduction capacitor on the high frequency noise of the REF102. $R_o$ is typically 7kΩ so the filter has a –3dB frequency of about 22Hz. The result is a reduction in noise from about 800µVp-p to under 200µVp-p. If further noise reduction is required, use the circuit in Figure 14.

FIGURE 5. Effect of 1µF Noise Reduction Capacitor on Broadband Noise ($f_{-3dB} = 1$MHz).
FIGURE 7. +10V Reference With Output Current Boosted to: a) ±20mA, b) +100mA, and c) $I_{L \text{ (TYP)}} +10mA, -5A$.

FIGURE 8. Strain Gauge Conditioner for 350Ω Bridge.

FIGURE 9. ±10V Reference.

FIGURE 10. Positive Precision Current Source.
FIGURE 11. Stacked References.

NOTES: (1) REF102s can be stacked to obtain voltages in multiples of 10V. (2) The supply voltage should be between 10n + 1.4 and 10n + 26 where n is the number of REF102s. (3) Output current of each REF102 must not exceed its rated output current of +10, -5mA. This includes the current delivered to the lower REF102.

FIGURE 12. ±5V Reference.

FIGURE 13. +5V and +10V Reference.


V_{\text{ref}} = \frac{(V_{\text{in1}} + V_{\text{in2}} + \ldots + V_{\text{inN}})}{N}

e_{\text{n}} = 5\mu\text{Vp-p (f = 0.1Hz to 1MHz)}

See AB-003 for more details.
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