



# High Power 53mm Silicon Controlled Rectifier

## 1300A / 2000V

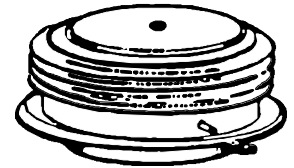
**C701**


The C701 Reverse Blocking Thyristor now has extended voltage blocking capability through unique multi-diffusion processing of 53 mm nominal silicon without sacrificing essential ratings and characteristics.

The C701 is designed specifically for phase control applications like DC motor control, power supplies, cycloconverters and load commutated inverters.

### FEATURES

- Optimized pilot gate for high di/dt rating
- Excellent withstand to high dv/dt voltage fronts
- Enhanced surge and I<sup>2</sup>t ratings for fuse coordination
- Glazed-fluted ceramic with metal — metal welded seal 1.0 in., 25.4 mm creepage  
1/8 in., 15.9 mm clearance



THYRISTOR (SCR) PRESSPAK

### MAXIMUM ALLOWABLE RATINGS

TYPE	REPETITIVE PEAK OFF-STATE AND REVERSE VOLTAGE, $V_{DRM}/V_{RRM}^1$ $T_J = -40^\circ\text{C to } +125^\circ\text{C}$	REPETITIVE PEAK OFF-STATE AND REVERSE VOLTAGE, $V_{DRM}/V_{RRM}^1$ $T_J = 0^\circ\text{C to } +125^\circ\text{C}$	TRANSIENT PEAK REVERSE VOLTAGE (NON-RECURRENT < 5 MILLISEC.), $V_{RSM}$ $T_J = -40^\circ\text{C to } +125^\circ\text{C}$
C701PA	1100 Volts	1200 Volts	1200 Volts
C701PB	1200	1300	1300
C701PC	1300	1400	1400
C701PD	1400	1500	1500
C701PE	1500	1600	1600
C701PM	1600	1700	1700
C701PS	1700	1800	1800
C701PN	1800	1900	1900
C701PT	1900	2000	2000
C701L	2000	2100	2100

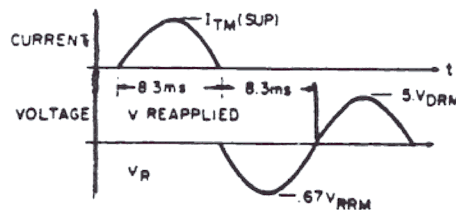
Average Forward Current, On-State @ $T_{case} = 70^\circ\text{C}$ , $I_T(AV)$ .....	1300A
Peak One-Cycle Surge On-State Current, $I_{TSM}$ 8.3ms .....	20KA
10.0ms .....	18KA
Maximum Repetitive Rate-of-Rise of Anode Current @ 1500V bias .....	100A/ $\mu\text{s}$
(Switching Rates $\leq 60$ Hz; snubber discharge $\leq 50A$ ; see required gate drive)	
I <sup>2</sup> t (for fusing) (at 8.3 milliseconds)	
Peak Gate Power Dissipation, $P_{GM}$ .....	200 W @ 40 $\mu\text{s}$ pulse
Average Gate Power Dissipation, $P_{G(AV)}$ .....	20W
Peak Reverse Gate Voltage, $V_{GRM}$ .....	20V
Peak Gate Current .....	15A
Storage Temperature, $T_{STG}$ .....	-40 $^\circ\text{C}$ to +150 $^\circ\text{C}$
Operating Temperature, $T_J$ .....	-40 $^\circ\text{C}$ to +125 $^\circ\text{C}$
Mounting Force Required .....	5000 - 6000 lb. 22.4 - 26.7 KN

### NOTE

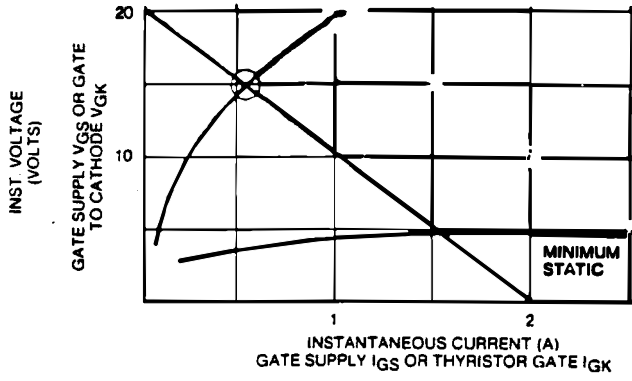
1. Half sine pulse. 10ms MAXIMUM pulse width, non repetitive  
Assume presspak mounted to heat dissipator of less than 0.3  $^\circ\text{C}/\text{W}$   
All ratings and tests in accordance with NEMA-EIA JEDEC Standard RS-397

## CHARACTERISTICS

TEST	SYMBOL	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Peak Reverse and Off-State Blocking Current	$I_{DRM}$ and $I_{RRM}$	-	10	15	mA	$T_j = +25^\circ\text{C}$ , $V = V_{DRM} = V_{RRM}$
Peak Reverse and Off-State Blocking Current	$I_{DRM}$ and $I_{RRM}$	-	45	65	mA	$T_j = +125^\circ\text{C}$ , $V = V_{DRM} = V_{RRM}$
Effective Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	-	-	.023	$^\circ\text{C/Watt}$	Junction-to-Case - Double Side Cooled (DC)
Critical Linear Rate-of-Rise of Forward Blocking Voltage (Higher values may cause device switching)	$dv/dt$	500	-	-	$\text{V}/\mu\text{sec}$	$T_j = +125^\circ\text{C}$ , $V_{DRM} = .80$ Rated, Gate Gate Open.
Holding Current	$I_H$	-	-	500	mAdc	$T_C = +25^\circ\text{C}$ , Anode supply = 20 Vdc. Initial On-State Current = 500 amps.
Latching Current	$I_L$	-	-	1.5	Adc	$T_C = +25^\circ\text{C}$ , Anode voltage = 24 Vdc. Load resistance 12 ohms max.
Delay Time	$t_d$	-	1.5	-	$\mu\text{sec}$	Switching From 300 Volts. 20 volt, 10 ohm Gate. 0.5 $\mu\text{sec}$ Rise Time, $T_j = 25^\circ\text{C}$
Gate Pulse Width Necessary to Trigger		-	-	10	$\mu\text{sec}$	0.5A, 15V minimum to support ratings
Gate Trigger Current nonoperational	$I_{GT}$	-	60	150	mAdc	$T_C = 25^\circ\text{C}$ , $V_D = 10$ Vdc, $R_L = 3$ ohms
		5.0	15	50		$T_C = +125^\circ\text{C}$ , $V_D = .5 \times$ Rated, $R_L = 1000$ ohms
Gate Trigger Voltage nonoperational	$V_{GT}$	-	2.5	4.5	Vdc	$T_C = 0^\circ\text{C}$ to $+125^\circ\text{C}$ , $V_D = 10$ Vdc, $R_L = 1000$ ohms
		.3	-	-		$T_C = +125^\circ\text{C}$ , $V_D = .5 \times$ Rated, $R_L = 1000$ ohms
Peak On-State Voltage	$V_{TM}$	-	-	1.21	Volts	$I_T = 1000\text{A}$ $T_j = 125^\circ\text{C}$
Circuit Commutated Turn-Off Time	$t_q$	-	125	250	$\mu\text{sec}$	(1) $T_C = +125^\circ\text{C}$ (2) $I_T = 1000$ Amps. (3) $V_R = 75$ Volts min. (4) 0.5 $V_{DRM}$ Reapplied (5) Rate-of-rise of reapplied forward blocking voltage = $50\text{V}/\mu\text{sec}$ . (linear) (6) Gate bias during turn-off interval, Duty cycle $\leq 0.01\%$
Suppressible Surge Current	$I_{TM(SUP)}$	-	18	-	KA	(1) $T_C = 115^\circ\text{C}$ (2) $V_R = .67 V_{DRM}$ (3) $.67 V_{RRM}$ Applied, 8.3 msec after completion of surge. (see waveforms below)



SUPPRESSIBLE SURGE CURRENT TEST



**Thyristor Gate Impedance**

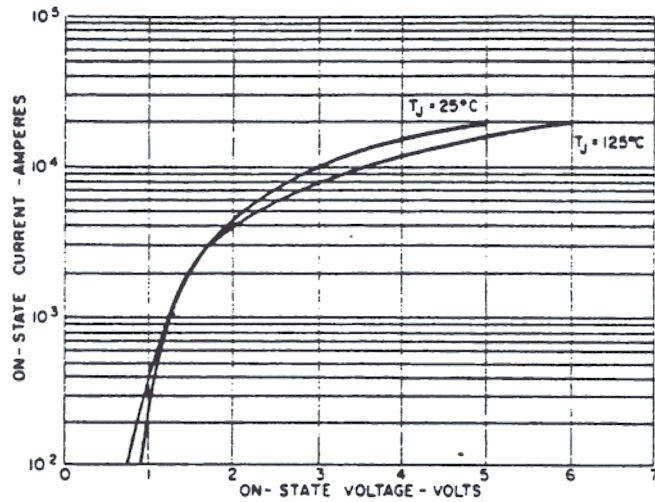
- This is enhanced by fast rising gate voltage, increasing anode bias and temperature.
- It is shown at a minimum for dc voltage, zero bias and low temperature.
- It is shown at a maximum for operating bias and recommended gate drive.

**Gate Supply**

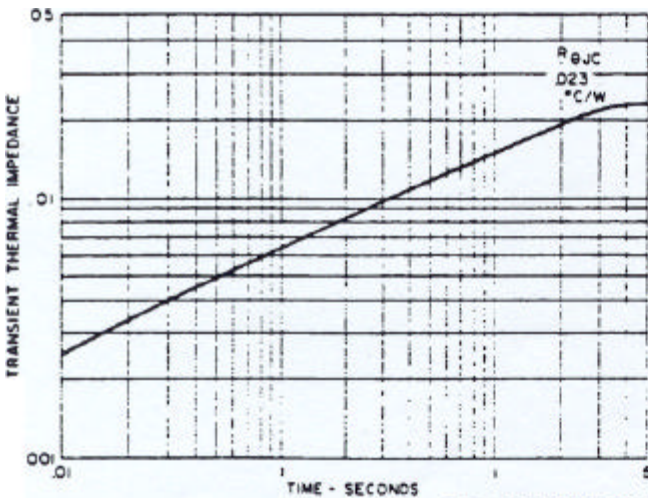
- The short circuit current rise time should be approximately  $0.5\mu s$  and the duration longer than the delay time expected for the thyristor.

**Minimum Acceptable Gate Current**

- The intersection of load line and gate characteristic (encircled) indicates the minimum value of actual current flowing into the gate that is required during the delay time interval needed for the published  $di/dt$  and snubber discharge ratings.



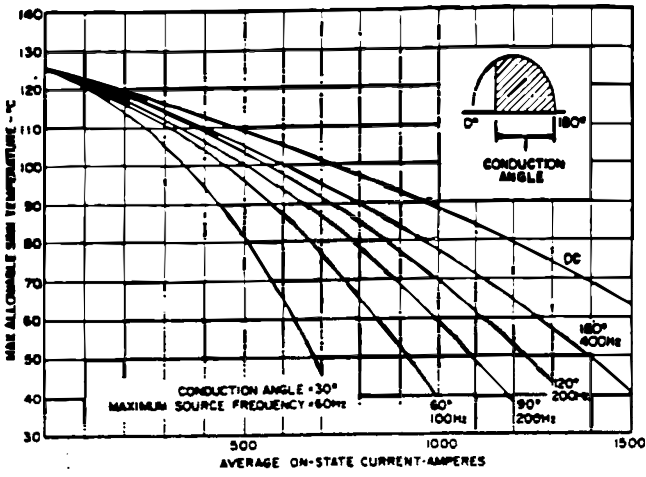
**MAXIMUM ON-STATE CHARACTERISTICS**



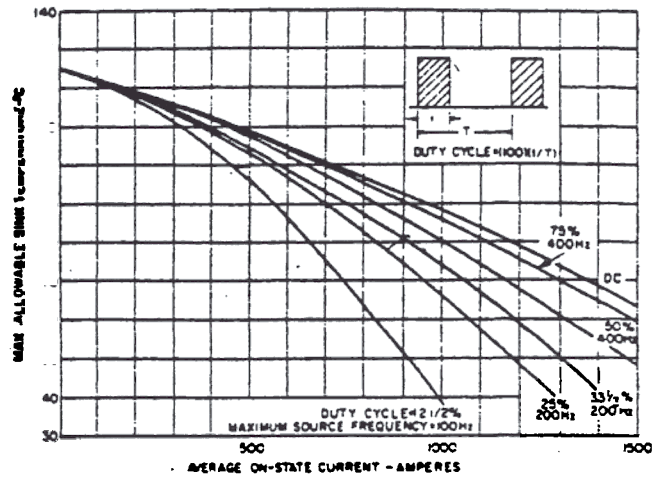
**TRANSIENT THERMAL RESISTANCE - JUNCTION-TO-HEATSINK**

**NOTES:**

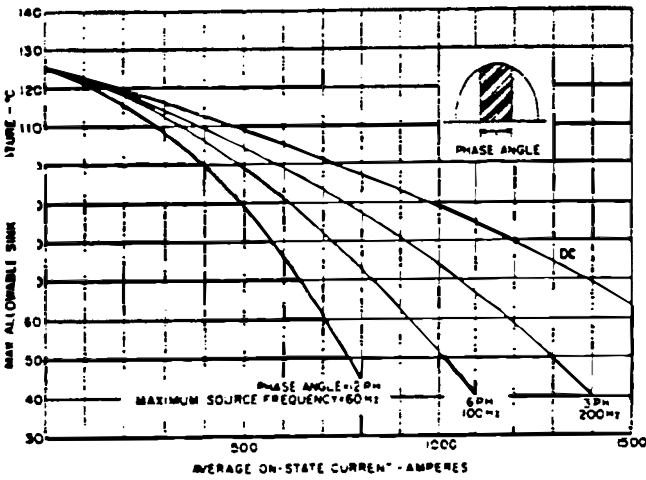
1. Add  $.006^{\circ}C/W$  to account for both case to dissipator interfaces when properly mounted; e.g.,  $R_{\theta JS} = .029^{\circ}C/W$ . See Mounting Instructions.
2. DC Thermal Impedance is based on average full cycle junction temperature. Instantaneous junction temperature may be calculated using the following modifications:
  - end of conducting portion of cycle
    - $120^{\circ}$  sq. wave add  $.0025^{\circ}C/W$  along entire curve
    - $180^{\circ}$  sq. wave add  $.0018^{\circ}C/W$  along entire curve
    - $180^{\circ}$  sine wave add  $.0010^{\circ}C/W$  along entire curve
  - end of full cycle
    - any wave, subtract  $.001^{\circ}C/W$  along entire curve.



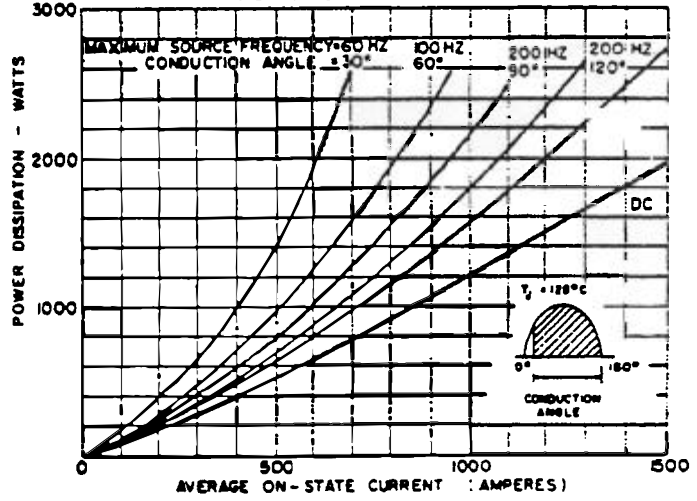
1. MAXIMUM ALLOWABLE HEATSINK TEMPERATURE FOR SINUSOIDAL CURRENT WAVEFORM - DOUBLE-SIDE COOLING



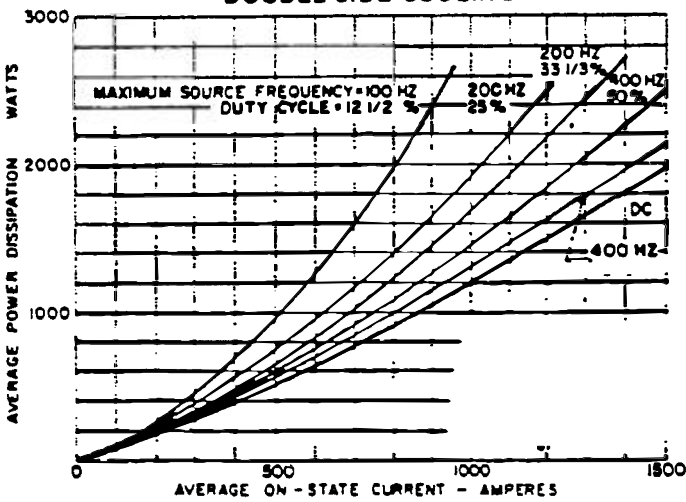
2. MAXIMUM ALLOWABLE HEATSINK TEMPERATURE FOR RECTANGULAR CURRENT WAVEFORM - DOUBLE-SIDE COOLING



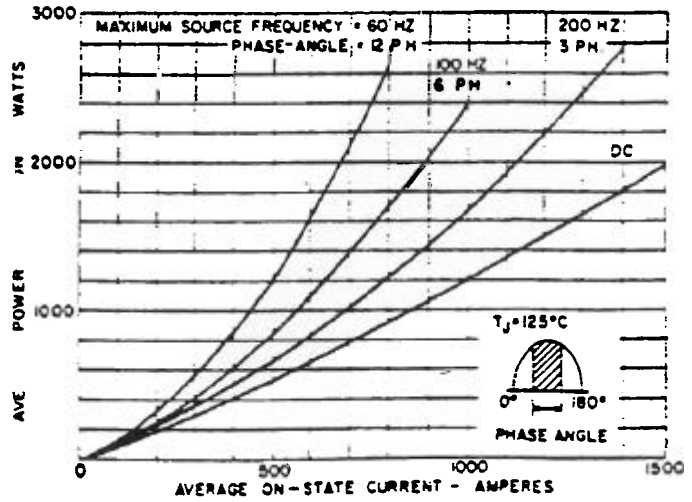
3. MAXIMUM ALLOWABLE HEATSINK TEMPERATURE - CIRCUIT PHASE CURRENT WAVEFORM - DOUBLE-SIDE COOLING



4. AVERAGE FORWARD POWER DISSIPATION FOR SINUSOIDAL CURRENT WAVEFORM



5. FORWARD POWER DISSIPATION FOR RECTANGULAR CURRENT WAVEFORM



6. AVERAGE FORWARD POWER DISSIPATION

