Let the first user among N users be the reference user without loss of generality. The probability density function (PDF) of the output of the mth square-law detector (Z_m) of an MFSK demodulator [4] with N interfering packets (users) is given by

$$P_{Z_m}(z_m) = \sum_{l=0}^{N-1} P_{Z_m}(z_m|l)P_h(N,l) \qquad m = 1,...,M \quad l = 0,...,N-1 \quad (1)$$

where $P_{Z_m}(z_m|l)$ is the conditional PDF of Z_m, l is the number of interfering packets which hit the M-ary sub-band of the reference user, and $P_h(N, l)$ is the probability that the l interfering packets hit the reference user. In eqn. 1, $P_{Z_m}(z_m|l)$ is given by

$$P_{Z_m}(z_m|l) = \sum_{l_0=0}^{l} P_l(z_m)\binom{l}{l_0}\left(\frac{1}{M}\right)^{l_0}\left(\frac{M-1}{M}\right)^{l-l_0} \quad (2)$$

where $P_l(z_m)$ is the PDF of the squared envelope of a sum of l random phase vectors given in [4] and l_0 ($\leq l$) is the number of users which hit the sub-band of the reference user; $P_h(N, l)$ is given by

$$P_h(N,l) = \binom{N-1}{l}\left(\frac{1}{q}\right)^{l}\left(1-\frac{1}{q}\right)^{N-1-l} \quad (3)$$

where, for the hop synchronous case, the probability that a reference user is hit by any other interfering user is given by $P_h = 1/q$.

For the reference user, it is assumed that the signal of the first filter among M filter banks of the MFSK demodulator is transmitted. The outputs of M filter banks, Z_1, ..., Z_M, can be regarded as i.i.d. random variables. After combining i packets, the symbol error probability is given by

$$P_s = 1 - P_c \quad (4)$$

where P_c is the probability of a correct decision given by

$$P_c = \int_{-\infty}^{\infty}\left[\int_{-\infty}^{z_1} P_{Z_2}(z_2,n_1)*P_{Z_2}(z_2,n_2)*\cdots*P_{Z_2}(z_2,n_i)dz_2\right]^{M-1} \cdot P_{Z_1}(z_1,n_1)*P_{Z_1}(z_1,n_2)*\cdots*P_{Z_1}(z_1,n_i)dz_1 \quad (5)$$

where $P_{Z_1}(z_1, n_i)$ is the PDF of Z_1 and is given by the same expression as eqn. 1 only with N replaced by n_i when i copies of a packet are present in the receiver.

For a slow Rayleigh fading with lognormal shadowing environment, the symbol error probability is given by

$$P_s' = \int_0^{\infty} P_s \cdot f_{\beta,s}(x)dx \quad (6)$$

where P_s is the symbol error probability for an AWGN channel and $f_{\beta,s}(x)$ is the combined probability density function (PDF) of Rayleigh fading with shadowing [3]. The detected error probability of an RS decoder is given by

$$P_E(N) = \sum_{j=\lfloor (n-k)/2\rfloor+1}^{n}\binom{n}{j}[P_s']^j[1-P_s']^{n-j} \quad (7)$$

where $\lfloor x \rfloor$ denotes the largest integer smaller than x.

The normalised packet throughput is defined as the average number of successfully received packets per packet transmission period and is given by

$$\eta = \left(\frac{N}{D_N}\right)\cdot\left(\frac{k}{n}\right)\cdot\left(\frac{1}{q}\right) \quad (8)$$

where D_N is the delay (the average number of packet transmissions for the successful reception of a single packet) with the N interfering packets, and is bounded by [5]

$$D_N \leq 1 + P_E(1) + P_E(2) + P_E(3) + \cdots \quad (9)$$

Simulation results and discussions: For the simulation examples, a standard deviation of lognormal shadowing σ_ξ = 8dB, a (63, k) RS code, 8-ary FSK modulation, number of frequency bins q = 128, uniform linear array with half wavelength antenna spacing and forgetting factor for the RLS algorithm 0.95 are assumed. The numbers of information symbols for the no-combining and the combining cases are chosen as k = 21 and k = 45, respectively, where the value of k is determined by the optimal code rate for achieving maximum throughput from extensive simulations. In the decoding of the RS code, bounded distance decoding (BDD) is used, so the received codeword is not decoded correctly if $e + 2t > n - k$ where t is the error correcting capability. In Fig. 2, the packet throughput against the number of interfering packets is shown for the various numbers of array elements with and without packet combining. The packet throughput is significantly increased by employing an adaptive antenna array and packet combining for a full range of numbers of interfering packets. The considerations in this Letter can be applied to the design of FH networks, and extended to the unslotted case.

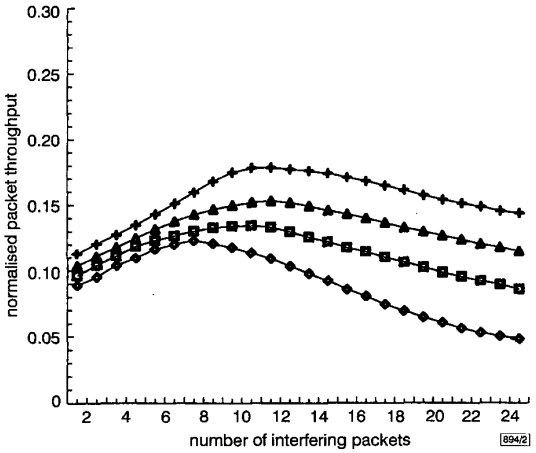

Fig. 2 *Packet throughput against the number of interfering packets*

—◇— no combining and single array
—□— no combining and 4 array
—△— combining and 4 array
—+— combining and 8 array

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4bit CLA-based conversion from redundant to binary representation for CMOS simple and multi-output implementations

G.A. Ruiz

New equations for converting a redundant number into its two's complement representation are presented. This enables converters to use conventional CMOS adder structures in dynamic logic, multi-output logic and differential logic. Static 4bit CLA circuits with a compact, regular, fast, simple and multi-output structure are described.

Introduction: The redundant binary representation is one of the signed-digit (SD) number representations proposed by Avizienis

[1]. It has a fixed radix of 2 and a digit set $\{0, 1, \bar{1}\}$, where $\bar{1}$ denotes -1. The redundancy introduced in this number system allows an SD number to be represented in more than one way. As a result, the addition of two SD numbers can be performed in a constant amount of time, independent of the word length (carry-free addition). Thus, the SD representation is especially useful for multi-operand addition. Practical high speed architectures of multipliers [2] and divisors [3] using the redundant binary representation have proved to be very suitable for VLSI implementation.

Because two's complement numbers are used in the external representation, the conversion between a two's complement number and a redundant number must be carried out. The conversion of a two's complement binary number into a redundant binary representation can be performed directly by changing the most significant digit 1 to $\bar{1}$. The inverse conversion can be made in a simple though not very efficient way by means of an adder. Different schemes for converting a redundant number into its two's complement representation have been proposed. In [4] a parallel converter was proposed based on a hybrid carry-lookahead/carry-select structure which is faster than the fastest known binary lookahead adder, but has a high area cost; a later improved modification is described in [5]. In [6] a new converter was presented based on a conventional carry-lookahead circuit using standard gates which requires less chip area and has a lower delay. Recently, a static CMOS circuit with a regular layout and structure similar to that required by standard carry-lookahead logic for adders has been proposed [9]. A converter specifically designed for multiplication schemes from MSB to LSB without carry propagation is described in [10] which is derived from the algorithm presented in [12].

This Letter presents new logic equations for converters which can be efficiently implemented in CMOS circuits. Converters based on adders designed in dynamic logic, multi-output logic and differential logic are now available, the resulting circuits being less complex and requiring a smaller number of transistors.

Conversion logic: The conversion of an n-digit redundant number $[X_{n-1}, X_{n-2}, ..., X_1, X_0]_{SD}$ ($X_i \in [\bar{1}, 0, 1]$) into its $(n + 1)$-bit two's complement binary number $[B_n, B_{n-1}, ..., B_1, B_0]_2$ from LSB to MSB can be efficiently performed by means of a convert-carry signal (C_i) [6]. Table 1 shows the conversion rules between the two representations of numbers. The i-digit of a redundant number is represented by two binary *bits* (S_i, D_i) with the encoding: $\{0, 1, \bar{1}\} = \{(0, 0), (0, 1), (1, 0)\}$.

Table 1 Conversion rules from redundant-binary into two's complement

X_i	S_i	D_i	C_i	$\bar{C}_i$	P_i	B_i	C_{i+1}	$\bar{C}_{i+1}$
0	0	0	0	1	1	0	0	1
	0	0	1	0	1	1	1	0
1	0	1	0	1	0	1	0	1
	0	1	1	0	0	0	0	1
$\bar{1}$	1	0	0	1	0	1	1	0
	1	0	1	0	0	0	1	0

From Table 1, the following equation can be easily derived:

$$C_{i+1} = S_i + \overline{D}_i C_i \tag{1}$$

Eqn. 1, used in previous converters [2, 6], cannot be efficiently implemented in CMOS iterative shared transistor structures. Applying Boolean algebra, this equation is transformed into

$$C_{i+1} = S_i + \overline{D}_i \overline{S}_i C_i = S_i + P_i C_i \tag{2}$$

In the same way, the complement carry is defined as

$$\overline{C}_{i+1} = D_i + \overline{S}_i \overline{C}_i = D_i + \overline{S}_i \overline{D}_i \overline{C}_i = D_i + P_i \overline{C}_i \tag{3}$$

with $C_0 = 1$ ($\overline{C}_0 = 0$).

Expanding eqns. 2 and 3 to 4 bits yields

$$C_4 = S_3 + P_3 S_2 + P_3 P_2 S_1 + P_3 P_2 P_1 S_0 + P_3 P_2 P_1 P_0 C_0 \tag{4}$$

and

$$\overline{C}_4 = D_3 + P_3 D_2 + P_3 P_2 D_1 + P_3 P_2 P_1 D_0 + P_3 P_2 P_1 P_0 \overline{C}_0 \tag{5}$$

The Boolean equation for B_i is

$$B_i = (S_i + D_i) \oplus C_i = \overline{P_i \oplus C_i} \tag{6}$$

where $B_n = C_n$.

Eqns. 2, 3 and 6 are identical to those used in conventional adders. The concept of P_i is similar to the propagate signal in a carry look-ahead (CLA) adder. Note that P_i propagates indistinctly the carry or its complement, making it easy to implement in differential logic. Moreover, P_i, S_i and D_i are mutually exclusive (note $P_i S_i = P_i D_i = 0$) which avoids logical faults (e.g. 'false' discharges) at output nodes in multi-output gates caused by OR-AND forms [7]. Consequently, converter design consists simply in adapting the CMOS structures developed for adders. The resulting circuits are less complex, as the converter equations are simpler and require fewer transistors for their implementation. Converters based on the popular (dynamic) Manchester carry chain or high speed structures developed in multi-output domino logic [7] are now available. Furthermore, the similarity between the definition of the carry and its complement in eqns. 2 and 3 enables the efficient implementation of converters in differential logic for self-timed circuits [8] or for pass-transistor design [11].

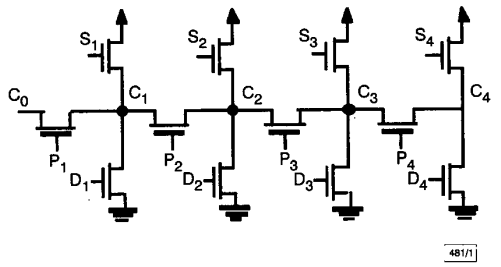

Fig. 1 *Static 4bit multi-ouput CLA*

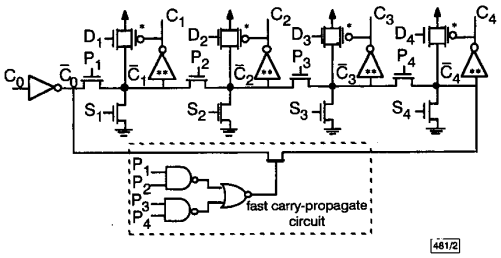

Fig. 2 *Improved static 4bit multi-ouput CLA with fast carry propagate circuit*

Fig. 1 shows a static 4bit CLA circuit based on eqn. 2 with a regular, fast, simple and multi-output structure which is more efficient than that presented in [9], since it enables all of the carries in one gate to be generated. This circuit has noise margin problems because the high level is lower than the supply voltage level by the threshold voltage of the pass transistors (P_i) and S_i transistors. Moreover, its speed is heavily dependent on the output load capacitance. Fig. 2 shows a more complete and improved version of this circuit based on eqn. 3. An input inverter is used to propagate the C_0 and output inverters to increase the fanout. Furthermore, the additional fast carry propagate circuit reduces the worst-case propagation time, turning on the bypass transistor if all carry propagate signals are true. The problems of noise margin are solved by means of the weak fedback PMOS transistors labelled * and non-symmetric output inverters labelled **. The transistor size for these inverters is obtained by shifting the midpoint voltage of the VTC to $(V_{DD} - V_{TN})/2$ using the following equation:

$$\frac{V_{DD} - V_{TN}}{2} = \frac{V_{DD} + V_{TP} + V_{TN}\sqrt{\beta_n/\beta_p}}{1 + \sqrt{\beta_n/\beta_p}} \tag{7}$$

Conclusion: The new converter equations presented in this Letter allow the use of adder structures such as carry look-ahead adders, carry skip adders and high speed adders [7] based on CMOS transistor sharing multi-output logic. In addition, the similarity between the equations of the carry and its complement enable the efficient implementation of converters in differential logic for self-timed applications and pass-transistor design.

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Modelling and measurement of radiated emissions from printed circuit boards

T.H. Ooi, S.Y. Tan and H. Li

An analytical model for the radiated emission from printed circuit boards based on multi-conductor transmission line theory is presented. The model includes the width of the ground plane, the thickness of the substrate and the size of the ground patch. Comparison of the theoretical results with measurements shows good general agreement.

Introduction: The radiated emission from printed circuit boards (PCBs) is mainly due to commonmode currents rather than differential-mode currents [1, 2]. Most transmission line (TL) and lumped-circuit models may be used to predict the differential-model currents, but these models inherently ignore the common-mode contributions. In this Letter we present a multi-conductor transmission line (MTL) model which gives the closed form expression of common-mode currents in terms of structure attributes and sources.

Formulation: Fig. 1 shows a typical PCB with a signal trace on one side of the substrate and a parallel ground plane connected with a ground patch on the other side. A three-conductor transmission line is formed by treating infinity as a conductor. Its equivalent circuit is shown in Fig. 2, where $Z_s = j\sqrt{[L_p/C_p]}\cot(\omega\sqrt{[L_pC_p]}L_1)$ is the input impedance of the ground patch and battery, ω is the angular frequency, L_1 is the length of the ground patch together with the battery, L_p and C_p are the per-unit-length inductance of the ground patch and the average per-unit-length capacitance of the ground plane and the battery with reference to infinity, $Z_{Fm} = j\omega L_{Fm}e^{-j\beta(L+L1)/2}$ is the impedance due to the magnetic coupling from the signal trace and the ground plane to the ground patch and the battery, L_{Fm} is their mutual inductance and β is the propagation constant of the field.

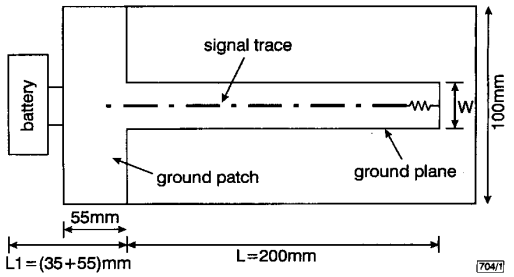

Fig. 1 *Structure of PCB for analysis*

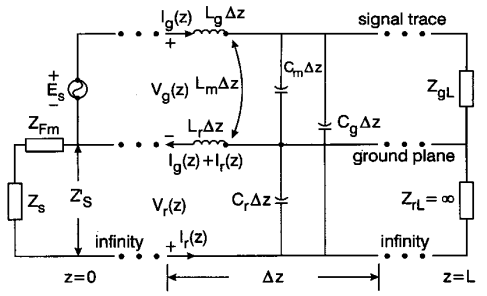

Fig. 2 *Equivalent circuit of MTL*

The MTL consists of the signal trace, the ground plane and infinity. Treating the ground plane as the reference, the MTL equations in the steady state (frequency domain) are given by

$$\frac{d^2V(z)}{dz^2} = ZYV(z) \tag{1}$$

$$\frac{d^2I(z)}{dz^2} = YZI(z) \tag{2}$$

where

$$V(z) = \begin{bmatrix} V_g(z) \\ V_r(z) \end{bmatrix} \quad I(z) = \begin{bmatrix} I_g(z) \\ I_r(z) \end{bmatrix}$$

$$Z = j\omega\begin{bmatrix} L_{11} & L_{12} \\ L_{21} & L_{22} \end{bmatrix} = j\omega\begin{bmatrix} L_g-2L_m+L_r & L_r-L_m \\ L_r-L_m & L_r \end{bmatrix}$$

$$Y = j\omega\begin{bmatrix} C_{11} & C_{12} \\ C_{21} & C_{22} \end{bmatrix} = j\omega\begin{bmatrix} C_g+C_m & -C_g \\ -C_g & C_r+C_g \end{bmatrix}$$

L_g and L_r are the per-unit-length self-inductances of the signal trace and the ground plane, respectively, L_m is their per-unit-length mutual inductance, C_g and C_r are the per-unit-length self-capacitance of the signal trace and the ground plane with reference to infinity and C_m is their per-unit-length mutual capacitance. All these per-unit-length parameters are calculated using numerical methods.

The common-mode current $I_r(z)$ and voltage $V_g(z)$ in most TLs are usually much smaller than the differential-mode current $I_g(z)$ and voltage $V_g(z)$. $I_r(z)$, from which common-mode radiation can be evaluated, is solved by ignoring the coupling from common-mode signals to differential-mode signals:

$$I_r(z) = \big((AV_g(0) + BZ'_sI_g(0))j\sin(\beta_2(L-z) + BI_g(L)(Z_r\cos(\beta_2 z) + jZ'_s\sin(\beta_2 z))\big)/ (Z_r\cos(\beta_2 L) + jZ'_s\sin(\beta_2 L)) - BI_g(z) \tag{3}$$

where

$$A = (L_{21}C_{11} - L_{22}C_g)/(L_{22}C_{22} - L_{11}C_{11})$$
$$B = (L_{21}C_{22} - C_gL_{11})/(L_{22}C_{22} - L_{11}C_{11})$$
$$Z_r = \sqrt{L_{22}/C_{22}} \qquad \beta_2 = \omega\sqrt{L_{22}C_{22}}$$

Fig. 3 shows the comparison between the measurements of Oka *et al.* [2] and our MTL model for the PCBs shown in Fig. 1. The dielectric constant and thickness of the PCB substrate are 4.7 and