PARALLEL-PIPELINED ARCHITECTURE FOR 2-D ICT VLSI IMPLEMENTATION

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ABSTRACT

The Integer Cosine Transform (ICT) has been shown to be an alternative to the DCT for image processing. This paper presents a parallel-pipelined architecture of an 8x8 ICT(10, 9, 6, 2, 3, 1) processor for image compression. The main characteristics of this architecture are: high throughput, low latency, reduced internal storage and 100% efficiency in all computational elements. The processor has been designed in 0.35-µm CMOS technology with an operational frequency of 300MHz.

Index Terms– integer cosine transform, multiplication free DCT, discrete cosine transform, image compression, parallel pipelined architectures, VLSI.

1. INTRODUCTION

Since the introduction of the Discrete Cosine Transform (DCT) several contributions have been made regarding fast algorithms and architectures for different applications. Of particular relevance are those describing 2D-DCT processors for image compression [1-5] and approximations to the DCT that are multiplication-free in order to reduce implementation complexity [6-7].

Although the DCT is the most widely used transform for image processing, other transforms have appeared over the last two decades which have both a smaller compression capacity and lower implementation costs [8-12]. Among these, the Integer Cosine Transform (ICT) [9-12] has been shown to be a promising alternative to the DCT [9] due to its implementation simplicity [13-14], similar performance and compatibility with the DCT. The ICT(10,9,6,2,3,1) has the advantage of not needing multipliers, as its kernel is a matrix on integers [13].

This paper describes a parallel-pipelined architecture of an 8x8 ICT(10, 9, 6, 2, 3,1) processor aimed at image compression. Based on a numerical strength reduction ICT algorithm, the architecture has been tailored to attain high throughput, having a low latency data flow that minimizes internal storage needs and keeps all computational elements at 100% efficiency. From this architecture, an 8x8 ICT processor, which meets the numerical characteristic requirements of the IEEE std. 1180-1990, has been designed using a 0.35-µm CMOS standard cell library. The circuit, with an area of 9.3 mm^2, has an operational frequency of 300MHz.

2. THE INTEGER COSINE TRANSFORM

The Integer Cosine Transform (ICT) was derived from the DCT through the concept of dyadic symmetry. The order-8 ICT kernel is

$$\mathbf{T} = \mathbf{K}\,\mathbf{J} \tag{1}$$

where **K** is the normalization diagonal matrix and **J** an orthogonal matrix defined as

$$\mathbf{J} = \begin{bmatrix} g & g & g & g & g & g & g & g \\ a & b & c & d & -d & -c & -b & -a \\ e & f & -f & -e & -e & -f & f & e \\ b & -d & -a & -c & c & a & d & -b \\ g & -g & -g & g & g & -g & -g & g \\ c & -a & d & b & -b & -d & a & -c \\ f & -e & e & -f & -f & e & -e & f \\ d & -c & b & -a & a & -b & c & -d \end{bmatrix} \tag{2}$$

whose elements are all integers and satisfy

$$a\,b = a\,c + b\,d + c\,d \tag{3}$$

$$a \geq b \geq c \geq d \quad \text{and} \quad e \geq f \tag{4}$$

There are many possible **J** matrices, and the corresponding ICTs are denoted as ICT(a, b, c, d, e, f); g is always 1.

3. DECOMPOSITION OF THE 1-D ICT

The 1-D ICT for a real input sequence **x**(n) is defined as

$$\mathbf{X} = \mathbf{T}\,\mathbf{x} = \mathbf{K}\,\mathbf{J}\,\mathbf{x} = \mathbf{K}\,\mathbf{Y} \tag{5}$$

where **X** and **x** are dimension-8 column matrices. Reordering the input sequence and the transform coefficients according to the rules

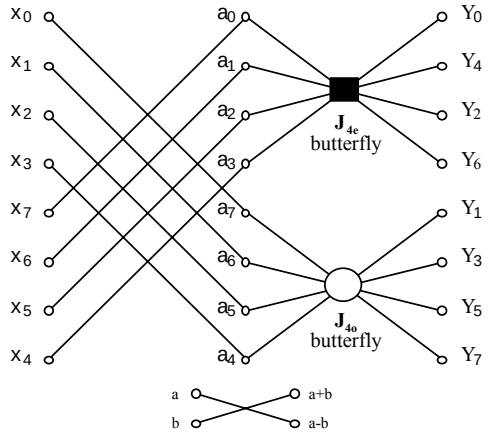

*Figure 1. **J** transform signal flow graph.*

$$\begin{cases} x'(n) = x(n) \\ x'(7-n) = x(n+4), \quad n \in [0,3] \end{cases} \tag{6}$$

$$\begin{cases} X'(m) = X(Br8[m]) \\ X'(m+4) = X(2m+1), \quad m \in [0,3] \end{cases} \tag{7}$$

where Br8[m] represents a bit-reverse operation of length 8, then the 1-D ICT can be expressed as

$$\mathbf{X'} = \mathbf{T_R}\ \mathbf{x'} = \mathbf{K_R}\ \mathbf{J_R}\ \mathbf{x'} = \mathbf{K_R}\ \mathbf{Y'} \tag{8}$$

The reordered integer ICT kernel is

$$\mathbf{J_R} = \begin{bmatrix} \mathbf{J_{4e}} & \mathbf{0} \\ \mathbf{0} & \mathbf{J_{4o}} \end{bmatrix} \begin{bmatrix} \mathbf{I_4} & \mathbf{I_4} \\ \mathbf{I_4} & \mathbf{-I_4} \end{bmatrix} \tag{9}$$

$\mathbf{I_4}$ being the dimension-4 identity matrix, and

$$\mathbf{J_{4e}} = \begin{bmatrix} g & g & g & g \\ g & -g & -g & g \\ e & f & -f & -e \\ f & -e & e & -f \end{bmatrix} \tag{10}$$

$$\mathbf{J_{4o}} = \begin{bmatrix} a & b & c & d \\ b & -d & -a & -c \\ c & -a & d & b \\ d & -c & b & -a \end{bmatrix} \tag{11}$$

Applying the decomposition rules defined in equations (6) and (7) to the $\mathbf{J_{4e}}$ matrix gives

$$\mathbf{J_{4e}} = \begin{bmatrix} \mathbf{J_{2e}} & \mathbf{0} \\ \mathbf{0} & \mathbf{J_{2o}} \end{bmatrix} \begin{bmatrix} \mathbf{I_2} & \mathbf{I_2} \\ \mathbf{I_2} & \mathbf{-I_2} \end{bmatrix} \mathbf{R_4} \tag{12}$$

where $\mathbf{R_4}$ is the reordering matrix of length 4, $\mathbf{I_2}$ is the dimension-2 identity matrix, and

$$\mathbf{J_{2e}} = \begin{bmatrix} g & g \\ g & -g \end{bmatrix} \tag{13}$$

$$\mathbf{J_{2o}} = \begin{bmatrix} e & f \\ f & -e \end{bmatrix} \tag{14}$$

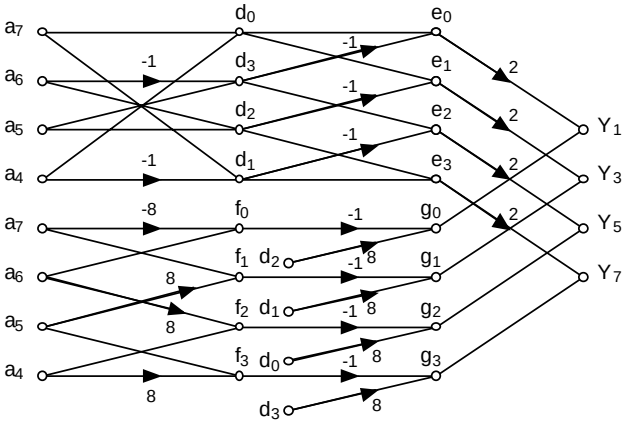

Figure 2. $\boldsymbol{J_{4o}}$ signal flow graph.

Figure 1 shows the signal flow graph obtained by applying the decomposition process to **J**(10,9,6,2,3,1). In this case, the $\mathbf{J_{4o}}$ matrix can be readily decomposed as

$$\mathbf{J_{4o}} = \begin{bmatrix} 10 & 9 & 6 & 2 \\ 9 & -2 & -10 & -6 \\ 6 & -10 & 2 & 9 \\ 2 & -6 & 9 & -10 \end{bmatrix} = \begin{bmatrix} 2 & 2 & -2 & 2 \\ 2 & -2 & -2 & 2 \\ -2 & -2 & 2 & 2 \\ 2 & 2 & 2 & -2 \end{bmatrix} + \begin{bmatrix} 0 & 8 & 8 & 0 \\ 8 & 0 & 0 & -8 \\ 8 & 0 & 0 & 8 \\ 0 & -8 & 8 & 0 \end{bmatrix} + \begin{bmatrix} -8 & 1 & 0 & 0 \\ 1 & 0 & 8 & 0 \\ 0 & 8 & 0 & 1 \\ 0 & 0 & 1 & 8 \end{bmatrix} - \begin{bmatrix} -8 & 1 & 0 & 0 \\ 1 & 0 & 8 & 0 \\ 0 & 8 & 0 & 1 \\ 0 & 0 & 1 & 8 \end{bmatrix} \tag{15}$$

in order to use only adding and shifting operations. The resulting signal flow graph for the $\mathbf{J_{4o}}$ transformation is shown in Figure 2.

4. DECOMPOSITION OF THE 2-D ICT

The 2-D ICT for a real input sequence **x** is defined as

$$\mathbf{X} = \mathbf{T}\ \mathbf{x}\ \mathbf{T}^t = \mathbf{K}\ \mathbf{J}\ \mathbf{x}\ \mathbf{J}^t\ \mathbf{K} = \mathbf{K}\ \mathbf{Y}\ \mathbf{K} \tag{16}$$

where **X** and **x** are 8x8 matrices. Reordering the input data and the transform coefficients applying the rules defined in (6) and (7) to both dimensions, the 2-D ICT can be expressed as

$$\mathbf{X'} = \mathbf{T_R}\ \mathbf{x'}\ \mathbf{T_R}^t = \mathbf{K_R}\ \mathbf{Y'}\ \mathbf{K_R} \tag{17}$$

where

$$\mathbf{Y'} = \begin{bmatrix} \mathbf{J_{4e}} & \mathbf{0} \\ \mathbf{0} & \mathbf{J_{4o}} \end{bmatrix} \begin{bmatrix} \mathbf{I_4} & \mathbf{I_4} \\ \mathbf{I_4} & \mathbf{-I_4} \end{bmatrix} \mathbf{x'} \begin{bmatrix} \mathbf{I_4} & \mathbf{I_4} \\ \mathbf{I_4} & \mathbf{-I_4} \end{bmatrix} \begin{bmatrix} \mathbf{J_{4e}^t} & \mathbf{0} \\ \mathbf{0} & \mathbf{J_{4o}} \end{bmatrix} \tag{18}$$

Figure 3 shows the signal flow graph obtained by applying the decomposition process to 2-D ICT(10, 9, 6, 2, 3, 1).

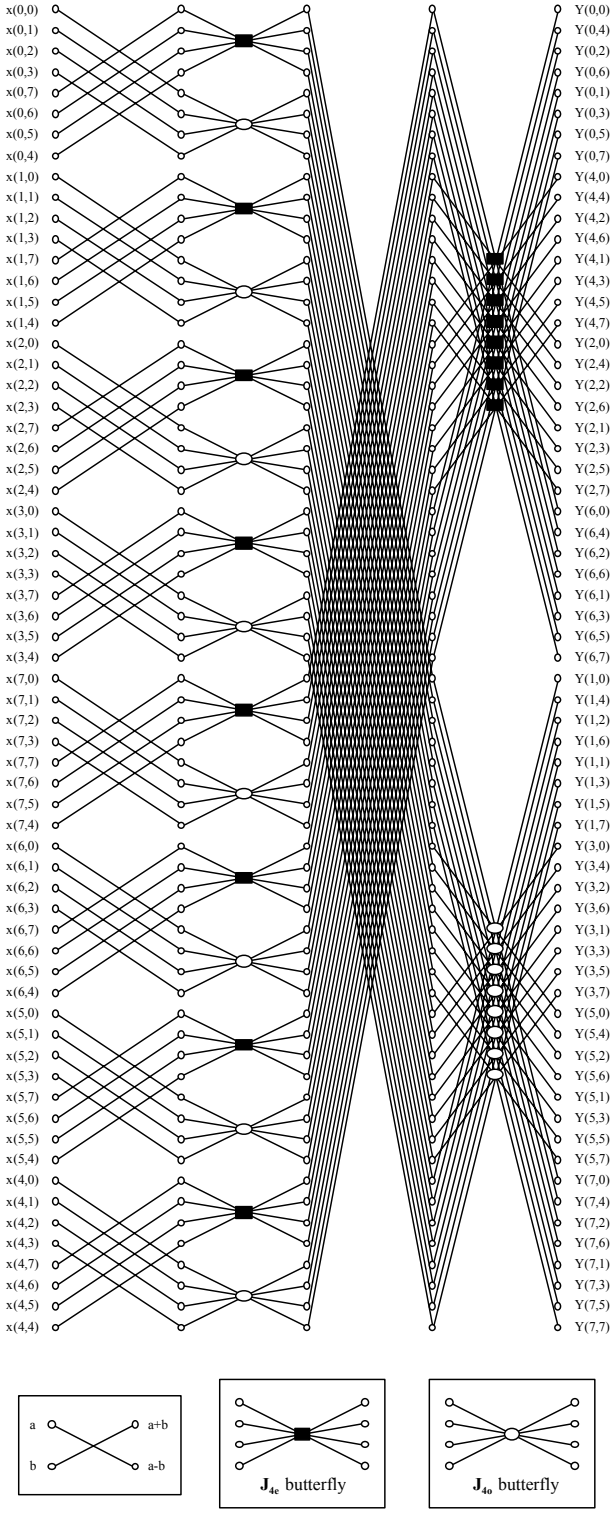

Figure 3. 8x8 ICT signal flow graph.

5. PARALLEL PIPELINED ARCHITECTURE WITH A THROUGHPUT RATE OF 1

The architecture shown in Figure 4 is based on a computing scheme that first obtains the 2-D **J** transform and then performs the normalization. This 2-D **J** transform is implemented using two 1-D **J**(10, 9, 6, 2, 3, 1) processors, sharing a register file for the storing of intermediate data. The input processor operates on each row of the input data block and stores the output coefficients on the register file. The second processor has as input the data stored on the register file -read in column (row) if they were written in row (column)- and produces the transform coefficients without normalization. A highly pipelined output multiplier performs the final normalization.

The 1-D **J** processor architecture has been conceived to implement efficiently the computation diagram of Figure 1 and to reduce the operating frequency to $f_s/2$, f_s which is the frequency of the input data. It has an input processor which performs the addition/subtraction of the input data pairs and two processors in parallel that carry out the transformations labeled $\mathbf{J_{4e}}$ (eq. 10) and $\mathbf{J_{4o}}$ (eq. 11). The output mixer circuit produces the un-normalized output coefficient sequence at a rate equal to the sampling frequency.

The input processor has a shift register of length 11 to store the input data, two multiplexers and an arithmetic unit having an adder and a subtractor in parallel. The arithmetic unit produces the input data for the $\mathbf{J_{4e}}$ and $\mathbf{J_{4o}}$ processors.

Figure 5 shows the $\mathbf{J_{4e}}$ processor, which has been derived from eq. (12). This processor contains an input data register, three intermediate data registers, two multiplexers, an arithmetic unit having an adder and a subtractor in parallel, and an output data multiplexer to order the coefficients. The multiplication by 3, implemented by shifting/adding, is pipelined with the subtraction.

The $\mathbf{J_{4o}}$ processor architecture has been conceived from the decomposition defined in eq. 15, avoiding the need for multipliers. As can be seen in Figure 6, this processor has an input data register, four intermediate data registers, eight multiplexers, four adders and one subtractor operating in parallel.

The computing efficiency of all processors is 100%.

Based on this architecture, an 8x8 ICT processor, meeting the numerical characteristic requirements of the IEEE std. 1180-1990, has been designed in 0.35-µm CMOS AMS technology using standard cell methodology. This circuit occupies an area of 9.3 mm^2 and has its operational frequency at 300MHz. The output multiplier has been implemented with fine grain pipeline architecture to make possible this high rate.

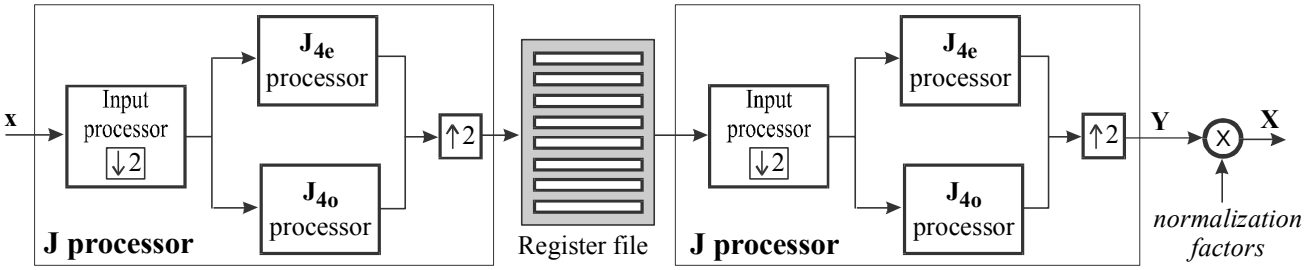

Figure 4. Architecture of 8x8 2-D ICT processor.

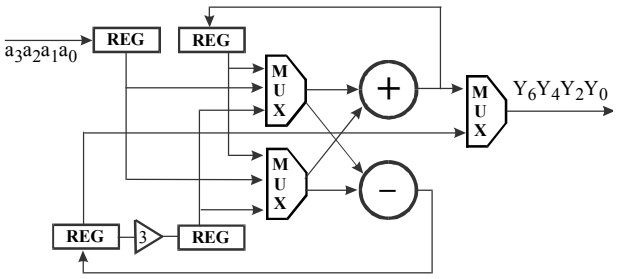

Figure 5. Architecture of J_{4e} processor.

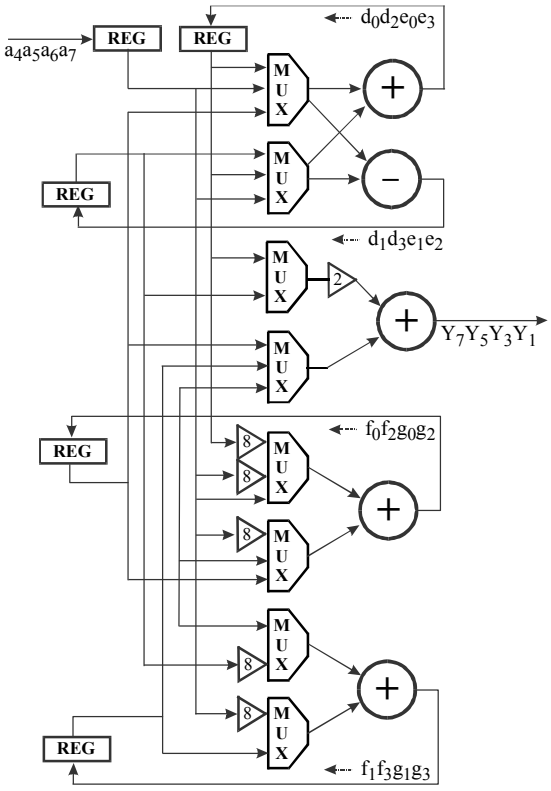

Figure 6. Architecture of J_{4o} processor.

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