New static multi-output carry lookahead CMOS adders

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Abstract: The paper presents new compact static 4-bit CMOS adders based on iterative shared transistor carry lookahead (CLA) units. The CLA units have a regular, fast, simple and multi-output static structure with a small number of transistors. Designs made in 1.0μm CMOS technology show that these adders reduce the silicon area and improve the timing and dynamic power performance compared with similar static adders.

1 Introduction

The adder is a key arithmetic component of most digital systems. Three characteristics are sought in the design of an adder: a regular structure, a fast logic evaluation and a compact circuit layout. Different kinds of adders which, to a greater or lesser extent, come close to these characteristics have been proposed: carry-ripple adders [1], carry-lookahead adders [2, 3], carry-skip adders [4, 5] and carry-select adders [6]. High-speed adder units based on the carry lookahead (CLA) principle remain dominant, since the carry delay can be improved by calculating the carries to each stage in parallel. The Manchester carry chain (MCC) is the most popular dynamic (domino) CLA, with a regular, fast and simple structure adequate for implementation in VLSI [2, 7, 8]. The recursive properties of the carries in the MCC have enabled the development of multi-output domino gates which have shown area and speed improvement with respect to single output ones [9, 10]. However, in some cases a static design of adders is required to perform an addition operation asynchronously. The efficiency of the MCC is lost when trying to transfer its structure to static logic. The static adders proposed up to now either present a rather irregular structure or require a high silicon area. In [11] a report has been made of a static CMOS 4-bit CLA adder in multi-output logic which substantially reduces the number of transistors with respect to a conventional schema. However, the simulation results have not shown any speed improvement, in contrast with the indications of the authors.

In this paper, some new static CMOS 4-bit adders based on the CLA structure of the MCC are presented. This CLA has a great topological regularity, small area and multi-output structure which allows efficient implementation in VLSI. For this reason, a new generate signal, N, has been defined which transforms the dynamic structure of the MCC into a static one and enables the properties of the latter to be exploited. A comparative analysis of the different static 4-bit CLA adders designed in CMOS 1.0μm technology highlights the considerable advantages of the proposed adders in terms of the total number of transistors, silicon area, dynamic power and speed.

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2 Preliminary concepts and previous work

The MCC is a fast and efficient dynamic (domino) circuit for CLA and carry calculation with a regular and simple structure ideal for high-speed adders. This circuit controls the carry-signal flow through two signals: the generate signal G and the propagate signal P so that the carry-out (C_i) for stage i can be expressed as

$$C_i = G_i + P_i C_{i-1} \tag{1}$$

where

$$G_i = A_i B_i \tag{2}$$

and

$$P_i = A_i \oplus B_i \tag{3}$$

where C_{i-1} is the carry-in and A_i and B_i are the input data.

Expanding this yields

$$C_i = G_i + P_i G_{i-1} + P_i P_{i-1} G_{i-2} + \cdots + P_i P_{i-1} \ldots P_1 C_0 \tag{4}$$

The sum is generated by

$$S_i = C_{i-1} \oplus A_i \oplus B_i = C_{i-1} \oplus P_i \tag{5}$$

Table 1 shows the truth table of the full adder carry-out. The operation time of the adder substantially depends on the carry evaluation time. The MCC generates all the carries in parallel using an iterative shared transistor structure with 'breakable' carry chain. Fig. 1 shows the implementation of this circuit in multi-output domino logic; in practice, the number of lookahead stages is limited to four in order to cut down on the number of series transistors. When *clk* is low, the output nodes are precharged by PMOS transistors. When *clk* is high, if $P_i = 1$, then the carry-in $\overline{C_{i-1}}$ is propagated; if $G_i = 1$, then C_i high is generated; and if $P_i = G_i = 0$, then C_i is dynamic, keeping low due to the precharge made by the PMOS transistors. The propagate and generate signals are mutually exclusive ($G_i P_i = 0$), which avoids the problem of 'false' discharges which are produced at the output nodes due to higher OR-

AND forms of multi-output gates. In Fig. 1, for example, the node $\overline{C_3}$ can be discharged through G_3 or P_3 but never through the higher output node $\overline{C_4}$ due to the exclusivity property of P_4 and G_4.

Table 1: Full adder carry-out

A_i	B_i	C_i	P_i	G_i	N_i
0	0	0	0	0	1
0	1	C_{i-1}	1	0	0
1	0	C_{i-1}	1	0	0
1	1	1	0	1	0

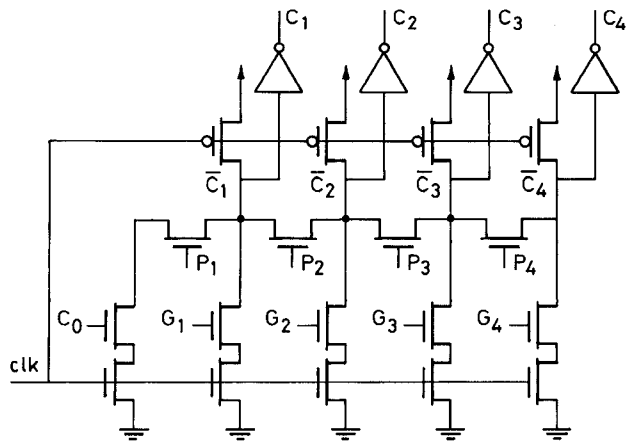

Fig. 1 *Four-stage MCC*

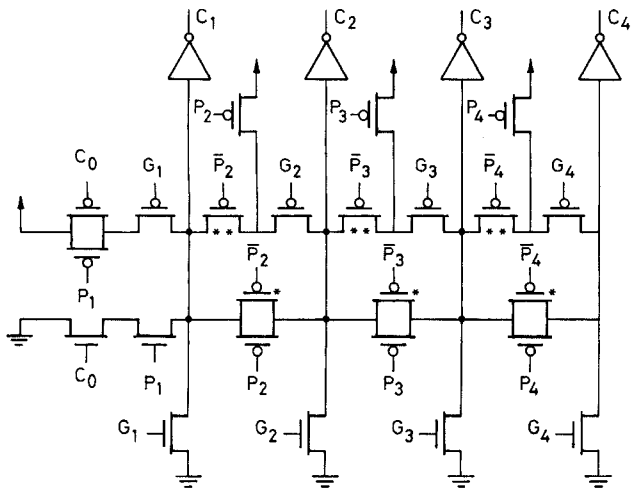

Fig. 2 *Static CMOS 4-bit CLA implementation in multi-output logic proposed in [11]*

When transferring the MCC structure to the static CMOS logic, the efficiency of the former is lost, since the PMOS logic tree does not verify the properties of the NMOS logic tree. The conventional implementation of a static CLA has to be carried out in independent gates for each of the output carries, with a consequent increase in size of the circuit. In [11], a static multi-output structure was proposed which significantly reduces the number of transistors from the conventional scheme. Fig. 2 shows this proposed 4-bit CLA CMOS implementation. The NMOS logic tree is similar to that of the MCC except for the parallel PMOS transistors labelled *, which improve the speed of the gate and provide full swing. Moreover, to avoid inconsistencies in the PMOS logic tree, the output nodes are isolated by means of the transistors labelled **. This CLA lacks a regular structure and presents redundancies, which can be eliminated to obtain a more compact circuit.

3 New static multi-output CLA adders

The dynamic shared transistor structure of the MCC is transformed into a static one by eliminating all the synchronisation transistors and annulling any possible dynamic states. The definition of a new generate signal, N_i (Table 1), eliminates the only dynamic state in the MCC, produced when $A_i = B_i = 0$. N_i is defined as

$$N_i = \overline{A_i + B_i} \tag{6}$$

The generate and propagate signals verify the following properties:

$$P_i G_i = P_i N_i = G_i N_i = 0 \tag{7}$$

$$P_i + G_i + N_i = 1 \tag{8}$$

Eqn. 7 indicates the mutually exclusive property between the propagate and generate signals, and eqn. 8 indicates that permanently one of these signals is high. The similitude between G_i and N_i is evident in the definition of $\overline{C_i}$, so that

$$\begin{aligned}\overline{C_i} &= \overline{G_i}(\overline{P_i} + \overline{C}_{i-1}) \\ &= \overline{G_i}(\overline{P_i} + \overline{C}_{i-1})(\overline{P_i} + P_i) \\ &= \overline{G_i}\,\overline{P_i} + \overline{G_i} P_i \overline{C}_{i-1}\end{aligned} \tag{9}$$

but

$$\overline{G_i} P_i = P_i \tag{10}$$

and

$$\overline{G_i}\,\overline{P_i} = \overline{A_i + B_i} = N_i \tag{11}$$

resulting in

$$\overline{C_i} = N_i + P_i \overline{C}_{i-1} \tag{12}$$

It can be observed that the definition of $\overline{C_i}$ is similar to that of C_i (eqn. 1), replacing N_i with G_i and C_{i-1} with $\overline{C}_{i-1}$. In both definitions P_i propagates indistinctly the carry-in or its complement. Eqns. 1 and 12 and the relation existing between the propagate and generate signals described in eqns. 7 and 8 enable two new static CLAs – one based on the propagation of the complementary carry-in and the other on the propagation of the noncomplementary carry-in, to be developed. Fig. 3 shows the first static CLA, labelled CLA–I, whose shared transistor structure is similar to that of the MCC. The signals $\overline{N_i}$ and G_i break the carry chain by generating a low ($\overline{N_i} = 0$) or high ($G_i = 1$) carry-out. P_i propagates the carry-in through NMOS pass-transistors with a high level lower than the supply voltage level by the threshold voltage. To improve the noise margins, an adequate gate width ratio between PMOS and NMOS in output inverters is 1.0 – less than that of ordinary CMOS inverters (1.5–2.5). Fig. 4 shows the dual version of the CLA–I, labelled CLA–II, which, based on the same principle, uses the symmetry existing between G_i and N_i. The carry input C_0 does not require either input or output inverters, since it propagates the carries without complementing. The connection of several CLA–IIs in cascade must be carried out through gates which limit the length of the chain of NMOS pass transistors. The small number of transistors (12 compared with the 22 of CLA–I) gives it a more compact structure. Nevertheless, its speed is very dependent on the output load capacitance which, together with the

problems of noise margin, conditions the type of gates which can be connected to the input and output carries; these problems are minimised in the CLA–I by means of the input and output inverters.

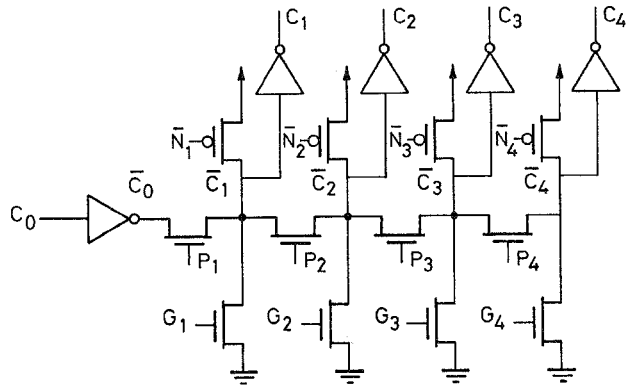

Fig. 3 *Four-stage CLA–I*

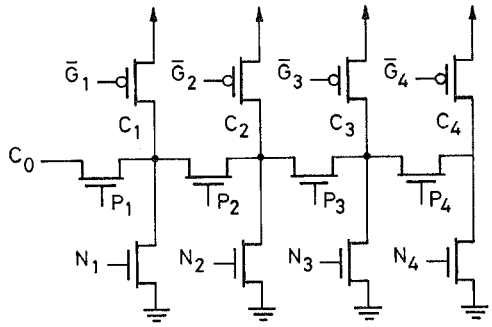

Fig. 4 *Four-stage CLA–II*

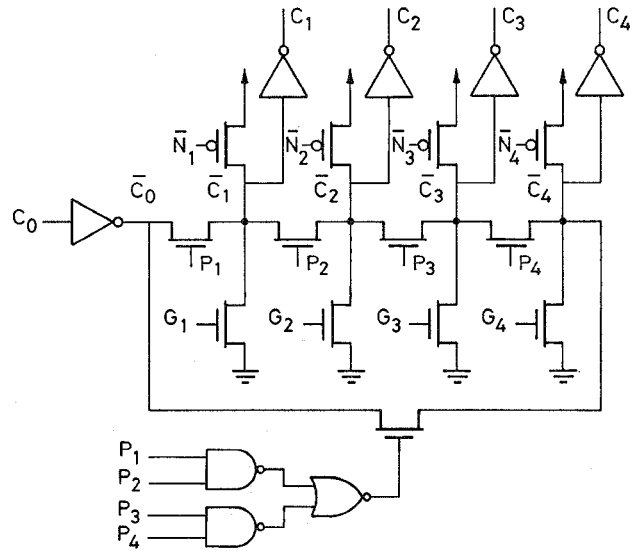

Fig. 5 *CLA–I with fast carry-propagate circuit*

The worst-case propagation time of the carry-out C_4 can be improved through the additional circuitry, as shown in Fig. 5; this same circuitry is valid for the CLA–II, connecting the bypass transistor between nodes C_0 and C_4. The bypass transistor turns on if all carry propagate signals are true and quickly transfers the carry-out C_4 after receiving the C_0. Thus, this arrangement should improve the overall speed of the adder because all P_is are generated in parallel and are evaluated simultaneously in this circuitry, significantly reducing the adder's critical delay time.

Figs. 6 and 7 show the structure of two 4-bit adders based on the CLA–I and CLA–II, respectively. They are composed of a G, P and N term generator which implements eqns. 2, 3 and 6, the static CLA unit and a sum block made up of EXOR gates (eqn. 5); the optimum number of stages may be calculated for a given technology by simulation.

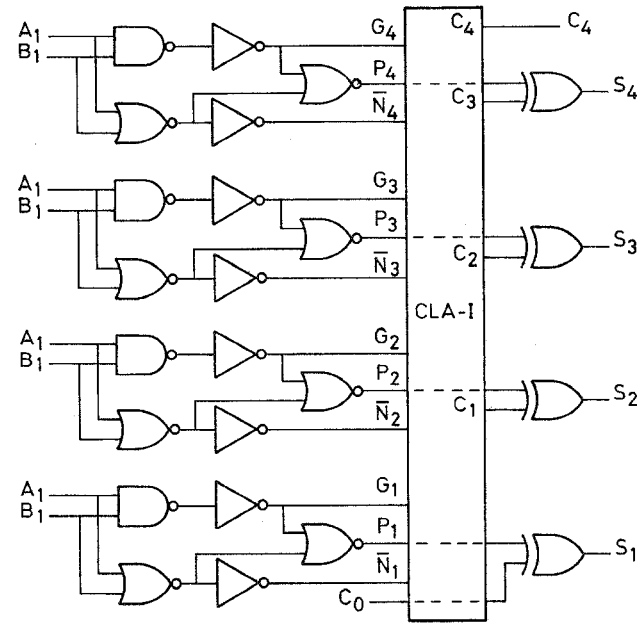

Fig. 6 *4-bit adder based on the CLA–I*

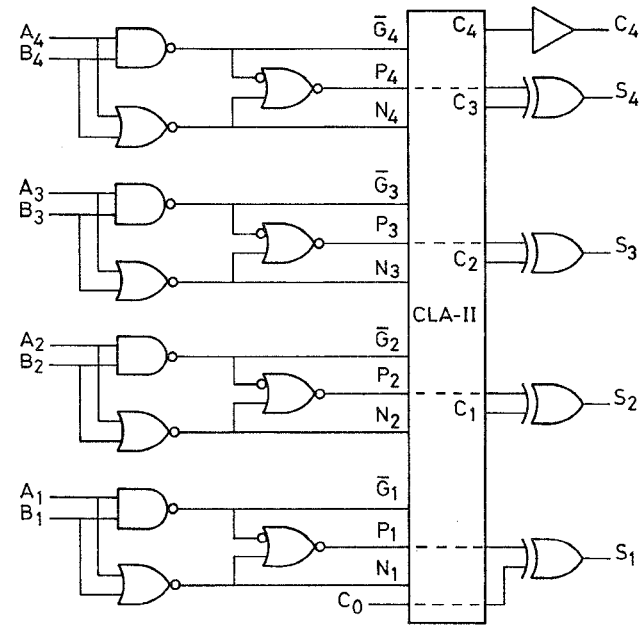

Fig. 7 *4-bit adder based on the CLA–II*

4 Results

Six static 4-bit adders with different CLA units have been designed using a double-metal 1.0μm CMOS technology and simulated with an HSPICE simulator at level 6, where V_{DD} = 5V, T = 25°C and C_L = 0.2pF. These adders are:

AddConv — conventional adder made up of a CLA with four independent gates for each of the carries

AddMO — adder with the multi-output CLA unit shown in Fig. 2

AddCLA–I adder shown in Fig. 6 with the CLA–I of Fig. 3

AddCLA–If AddCLA–I with the fast carry-propagate circuit shown in Fig. 5

AddCLA–II adder shown in Fig. 7 with the CLA of Fig. 4

AddCLA–IIf AddCLA–II with the fast carry-propagate circuit of Fig. 5.

Simulated results allow three different time types to be obtained: tp_{wc}, tp_{C0} and tp_{C1}. tp_{wc} is the worst-case propagation time, which is measured with the input operands $A = 0{\times}F$, $B = 0{\times}0$ and $C_0 = 1$. tp_{C1} and tp_{C0} are the propagation times of the carry-in C_0 throughout the carry chain. These provide a speed measurement for these adders when several are connected in the ripple-carry configuration. These times are calculated with the input operands $A = 0{\times}F$, $B = 0{\times}0$ fixed ($P_i = 1\ \forall i$) switching C_0 from 0 to 1 (tp_{C1}) and from 1 to 0 (tp_{C0}).

Table 2 summarises the characteristics and simulated results. It shows the size of the layout (in μm^2), the number of partial transistors in the CLA unit and the totals of the full adder, the dynamic power consumption at 1MHz, and the propagation times described previously. As expected, the conventional AddConv requires a greater number of transistors and, thus, a greater area of occupation. The tp_{wc} is 3.04ns and the power is very close to 1mW. The rest of the adders will be compared with the data from the AddConv. In contrast with that reported in [11], the AddMO does not significantly reduce the propagation times despite the reduction in area and power. This is due to the increase in capacitive loading in the internal nodes of the multi-output CLA unit which increases the gate propagation times. The ADDCLA–I slightly improves the tp_{wc} but substantially reduces the tp_{C1} and tp_{C0}. Better results are obtained in the fast version, AddCLA–If, with an important reduction in propagation times. The most efficient adder, both in terms of speed and area, is the AddCLA–II, which reduces all the parameters: area (69%), power (78%), tp_{wc} (89%), tp_{C1} (59%) and tp_{C0} (47%). Its fast version has carry propagation times below ns, which makes it ideal for high-speed applications.

Table 3 shows the dynamic power consumption and tp_{wc} of the previous adders in 32-bit ripple carry configuration. The simulation results show the substantial speed increase of the proposed adders, which can reach up to 52% (AddCLA–IIf). This is because the CLA–I or CLA–II units have reduced carry propagation times, which improve the overall performance of the adder.

Table 3: Simulation results of 32-bit adders in ripple carry configuration

	Power	tp_{wc}
AddConv	6.8	20.1
	(1.00)	(1.00)
AddMO	6.1	19.5
	(0.90)	(0.97)
AddCLA–I	5.9	16.0
	(0.87)	(0.80)
AddCLA–If	6.0	11.9
	(0.88)	(0.59)
AddCLA–II	5.5	14.6
	(0.81)	(0.73)
AddCLA–IIf	5.9	10.5
	(0.87)	(0.52)

5 Conclusion

In this paper, some new compact static 4-bit CMOS CLA adders are presented. These adders use iterative shared transistor CLA units whose structure is based on the popular dynamic (domino) Manchester carry chain (MCC). The static versions of the MCC have been attained by eliminating the synchronisation transistors and introducing a new generate signal (N) which eliminates the dynamic states. As a result, two new CLAs have been defined, labelled as CLA–I and CLA–II, which are characterised by their great topological regularity, small area and multi-output structure and whose worst-case propagation time can be improved by additional circuitry. Designs made in 1.0μm CMOS technology show that the proposed adders are more efficient in terms of speed, power and area compared with other static adders. Finally, the similitude between CLA–I and CLA–II and the MCC enable some of the latter's properties to be exploited. Thus, adders based on MCC, such as those presented in [7, 8], can easily be transformed to static ones in those applications which require an additional operation to be performed asynchronously.

Table 2: Characteristics of 4-bit adders with different CLA units

	Area	TCLA	Tall	Power	tp_{wc}	tp_{C1}	tp_{C0}
AddConv	32752	56	152	0.995	3.04	2.38	2.99
	(1.00)	(1.00)	(1.00)	(1.00)	(1.00)	(1.00)	(1.00)
AddMO	26835	32	128	0.93	3.02	2.37	2.73
	(0.82)	(0.57)	(0.84)	(0.90)	(0.99)	(1.00)	(0.91)
AddCLA–I	26375	22	126	0.865	2.82	1.53	1.59
	(0.81)	(0.39)	(0.83)	(0.87)	(0.93)	(0.64)	(0.53)
AddCLA–If	28337	35	139	0.91	2.59	1.07	1.25
	(0.87)	(0.63)	(0.91)	(0.91)	(0.85)	(0.45)	(0.42)
AddCLA–II	22440	12	112	0.78	2.72	1.40	1.41
	(0.69)	(0.21)	(0.74)	(0.78)	(0.89)	(0.59)	(0.47)
AddCLA–IIf	26272	25	125	0.83	2.48	0.88	0.80
	(0.80)	(0.45)	(0.82)	(0.83)	(0.82)	(0.37)	(0.27)

Area: size of layout in μm^2. *TCLA*: number of transistors of the carry lookahead stage. *Tall*: total number of transistors. *Power*: dynamic power consumption (in mW) at 1MHz. tp_{wc}: worst case propagation time (in ns). tp_{C1}: propagation time (in ns) of the carry-in high. tp_{C0}: propagation time (in ns) of the carry-in low

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